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Introducing SPECS: Scalable Photonic Event-driven Circuit Simulator

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Abstract *We present SPECS, a SystemC-based tool for fast, fs-accurate large-scale photonic circuit simulation. Through its event-driven nature, SPECS excels in sparse activity applications like neuromorphic computing. Even in unfavorable scenarios, it is faster than other simulators by orders of magnitude. ©2023 The Author(s)*

Introduction

As photonic technology takes on an increasingly significant role in various applications in telecommunications, sensing, and computing^{[1],[2]}, accurate and efficient simulation tools become essential for designing, verifying, and optimizing photonic components and systems^[3].

Photonic simulations rely on a multi-level abstraction methodology similar to the one prevalent in electronics^[4], and in fact re-purposes many tools from the electronic design automation (EDA) portfolio^{[5]-[7]}. At the device level, 2D/3D electromagnetic simulations provide detailed information about the behavior of individual components. This information, crossed with device measurements, is used to create simplified device models for use in circuit simulators such as Lumerical™ Interconnect^[8], Luceda Caphe (now part of the IPKISS framework)^[9], or Photontorch^[10]. Finally, system designers can simplify circuit behavior into system-level metrics (e.g., bandwidth, latency...) to perform very large-scale analyses^[11]. These methods have been proven useful, but result in prohibitive computational costs (at circuit level) or modelling efforts (at system level) when designing large-scale photonic circuits, calling for an intermediate abstraction level between circuit and system, still inexistent in photonics^[12].

In electronics, industry standards for hardware description languages (HDL)^[13] were instrumental to enabling the design of large systems. These standards were further improved with analog and mixed-signal (AMS) extensions to provide both continuous-time and event-driven modeling primitives in a single package^[14]. In event-driven solvers, components are simulated only when necessary, significantly reducing computational

costs and enabling more efficient analysis of large-scale systems, without degrading temporal accuracy. This approach seems particularly well-suited for optical systems, which often exhibit temporally and/or spatially sparse activity^[15], owing to the scale difference between the speed of signals and the bandwidth of supporting electronics. While there are priors for event-driven simulation of photonic circuits^{[16]-[18]}, they focus on the interconnect layer and abstracted system-level metrics.

In this contribution, we introduce SPECS (Scalable Photonic Event-driven Circuit Simulator)^[19], an open-source simulation tool that leverages the event-driven paradigm to overcome performance limitations of traditional time-driven simulation methods. We first present the rationale between our approach and brief implementation details of SPECS. We then demonstrate the effectiveness of SPECS by studying a Coupled-Resonator Optical Waveguide (CROW) circuit and compare it with Interconnect and Photontorch (PT).

Proposed Approach

SPECS is built upon the SystemC framework, a widely adopted hardware description language (HDL) and simulation library for system-level design^[20]. By utilizing SystemC, we facilitate the integration of SPECS with other system-level design tools and enable efficient co-simulation of photonic and electronic subsystems.

For circuit description, SPECS employs SPICE-like netlists, standard in electronic circuit simulators. This choice ensures ease of integration with a broad range of existing EDA tools and allows designers to leverage their knowledge and experience. Furthermore, this approach enables hier-

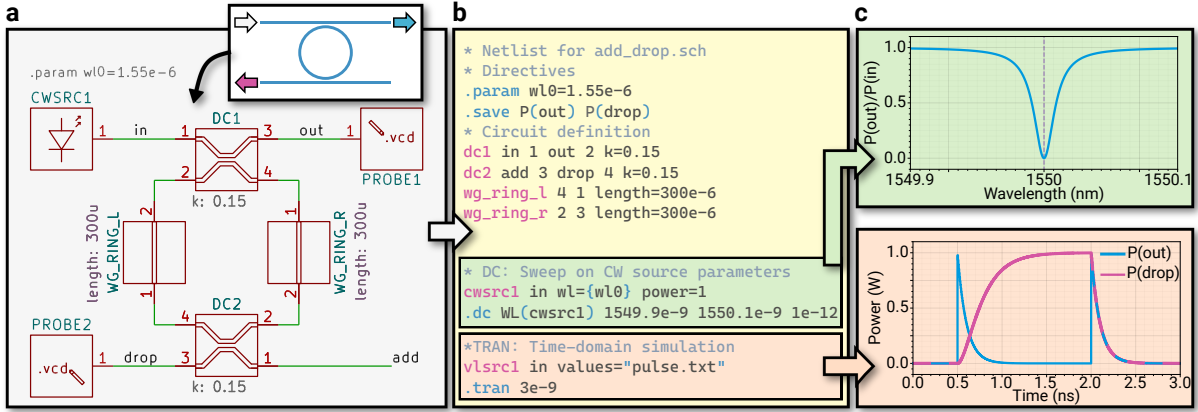


Fig. 1: Example design and simulation flow: (a) schematic description of the circuit, (b) the corresponding SPECS netlist, (c) frequency- and time-domain simulations of the circuit.

archical descriptions of photonic circuits, simplifying the design process and facilitating the co-simulation of complex systems.

While the current implementation of SPECS focuses on event-driven simulation, the framework can be extended to support mixed-mode simulations for cases where non-linear effects impose a more detailed analysis or, inversely, used to extend existing time-driven frameworks. Mixed-mode simulations would enable a more comprehensive coverage of various photonic circuit scenarios while still benefiting from the efficiency advantages of event-driven simulations.

A typical use of SPECS is shown in Figure 1. Existing tools, here KiCAD^[21], can be adapted to edit circuit schematics and generate a SPECS netlist, which can be used to perform frequency- or time-domain simulations.

Implementation Details

SPECS, like other photonic circuit simulators, adopts a "baseband" approach and represents optical signals by a complex field amplitude $\underline{E}(t)$ and a carrier wavelength λ_0 . Waveforms are reduced to a sequence of square pulses which in turn are decomposed into at most two "events", as shown in Figure 2a. It should be noted that event-driven simulation is naturally more suited to digital waveforms than continuously varying ones. When a circuit component receives an event, it calculates the corresponding outputs and schedules their emission based on component-specific delays as illustrated in Figure 2b.

SPECS defines many basic components, such as waveguides, couplers, phase-shifters, generic S-matrix devices, as well as arbitrary sources and probes. The implementation of these components is straightforward and functionally equivalent to other circuit simulators^[10]. New compo-

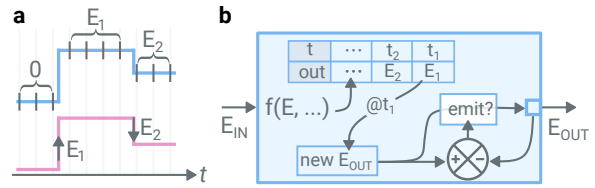


Fig. 2: (a) Digital signals are inefficiently represented in time-driven (top) simulators compared to event-driven (bottom) ones and (b) architecture of a unidirectional 2-port device in SPECS.

nents can be added by modifying the C++ source code or using a generic Python module for fast prototyping.

For purely feedforward circuits with digital inputs, SPECS approaches the optimal simulation time by design. For circuits involving feedback, it can still perform very well, provided that the balance between accuracy and runtime is chosen wisely. Several cursors are available for a user to tune the accuracy of simulations:

- *Temporal resolution* — sets the precision with which events are resolved. Decreasing resolution can greatly reduce simulation time, but will lower the precision of the final waveforms by masking what happens between events.
- *Absolute and Relative tolerance* — relax precision constraints by specifying a threshold below which small changes do not need to be emitted by devices. Without them, events representing infinitesimal changes in field values could propagate indefinitely in circuits with feedback. These should not be conflated with similarly named settings of time-driven simulators which, even though they share similar goals, typically control the time-step of the solver.

Lastly, both frequency-domain simulation and impulse-response calculation constitute special use-cases of SPECS and can be performed easily and efficiently without external software.

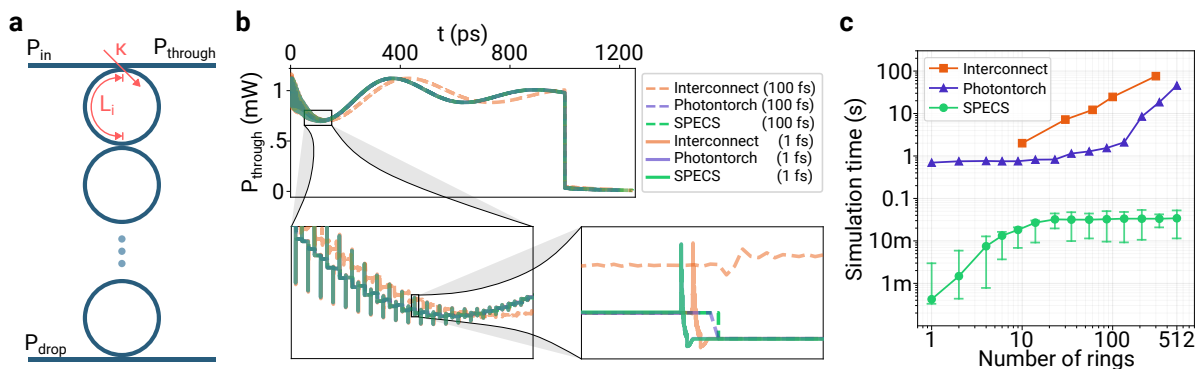


Fig. 3: Benchmark results (a) architecture of the CROW circuit used for benchmarking, (b) time-domain results for the same CROW ($N = 3$) on all simulators, at 100 fs and 1 fs (c) single-threaded CROW simulation times at 100 fs.

Results and Discussion

To evaluate the performance of SPECS, we studied a CROW circuit, shown in Figure 3a, made up of N chained ring resonators. This circuit is composed of one source emitting 1 mW, 1 ns pulses at 500 MHz, $2N$ waveguides with lengths $L_i = (33.2 \pm 5.0) \mu\text{m}$ sampled from a normal distribution, and $N + 1$ directional couplers with $\kappa = 0.15$ power cross-coupling ratio. Simulations were run on a single thread using a modern laptop powered by an Intel i7-1165G7 2.8 GHz CPU and 16 GB of RAM. Interconnect, PT and SPECS were all used as-is, with no platform-specific or circuit-specific tuning. SPECS' absolute and relative tolerances were respectively set to 10^{-8} V m^{-1} (0.1 fW) and 0.01 %.

We first verify our benchmarking environment by comparing the *through* response for $N = 3$ and very long delays ($L \approx 350 \mu\text{m}$). Results, presented in Fig. 3, show that Interconnect surprisingly did not match the response yielded by both PT and SPECS at 100 fs resolution. At 1 fs resolution, all simulations yielded nearly identical results, with pair-wise root-mean-square errors below $\sim 3 \mu\text{W}$, although SPECS was $6290\times$ (resp. $5090\times$) faster than PT (resp. Interconnect).

Finally, we turn to CROW circuits with up to $N = 512$ rings. In PT and Lumerical, we simulate for a duration of 3 ns (30000 timesteps at 100 fs). In SPECS, we instead simulate 10 equally-spaced 1 ns pulses (20 ns) and normalize the results to accurately capture the effect of events continuing to propagate beyond the initial duration and accumulating with subsequent pulses. Execution times for 3000 timesteps (300 ps), averaged over 100 runs for SPECS, are shown in Figure 3c. The whiskers in Figure 3c show the extrema measured for SPECS, due to the random sampling of waveguide lengths, illustrating the circuit-dependent variability in simulation times.

Although CROWS constitute an unfavorable

scenario for event-driven simulators, SPECS' performance remained order of magnitudes better than PT and Interconnect, in part because beyond $N \sim 20$, simulation time saturates around 40 ms due to losses preventing any meaningful signal (according to SPECS' tolerances) to propagate too far in the CROW. This native input dependent optimization is precisely what sets it apart from the state of the art.

We were not able to independently run a GPU-accelerated version of PT, but reported performances for this use-case^[10] are still an order of magnitude slower than SPECS running on a single thread.

Conclusions

Event-driven photonic simulation can be a powerful tool, and likely the next step for simulating large photonic circuits driven by digital waveforms, or exhibiting sparse activity.

We showed that our implementation outperforms off-the-shelf tools by a significant margin in terms of simulation speed while offering functionally similar accuracy. In particular, its performances scale very well with circuit size due to its naturally frugal simulation approach.

It is important to note that different simulators serve different purposes. For example, SPECS cannot efficiently optimize circuits through back-propagation like Photontorch does. Additionally, mixed-mode simulations will be necessary to cover more complex circuits.

Finally, through SystemC and a versatile netlist interface, SPECS can enable co-simulation of computing cores and photonic accelerators, or be integrated into other simulation platforms.

Acknowledgments

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References

- [1] B. Jalali and S. Fathpour, "Silicon Photonics", en, *Journal of Lightwave Technology*, vol. 24, no. 12, pp. 4600–4615, Dec. 2006, ISSN: 0733-8724. DOI: 10.1109/JLT.2006.885782.
- [2] D. Thomson, A. Zilkie, J. E. Bowers, *et al.*, "Roadmap on silicon photonics", en, *Journal of Optics*, vol. 18, no. 7, p. 073003, Jul. 2016, ISSN: 2040-8978, 2040-8986. DOI: 10.1088/2040-8978/18/7/073003.
- [3] L. Chrostowski and M. Hochberg, *Silicon Photonics Design*, en. Cambridge: Cambridge University Press, 2015, ISBN: 978-1-316-08416-8. DOI: 10.1017/CB09781316084168.
- [4] M. U. Khan, Y. Xing, Y. Ye, and W. Bogaerts, "Photonic Integrated Circuit Design in a Foundry+Fabless Ecosystem", en, *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 25, no. 5, pp. 1–14, Sep. 2019, ISSN: 1077-260X, 1558-4542. DOI: 10.1109/JSTQE.2019.2918949.
- [5] Y. Ye, T. Ullrick, W. Bogaerts, T. Dhaene, and D. Spina, "SPICE-Compatible Equivalent Circuit Models for Accurate Time-Domain Simulations of Passive Photonic Integrated Circuits", en, *Journal of Lightwave Technology*, vol. 40, no. 24, pp. 7856–7868, Dec. 2022, ISSN: 0733-8724, 1558-2213. DOI: 10.1109/JLT.2022.3206818.
- [6] P. Martin, F. Gays, E. Grellier, A. Myko, and S. Menezo, "Modeling of silicon photonics devices with Verilog-A", en, in *2014 29th International Conference on Microelectronics Proceedings - MIEL 2014*, Belgrade, Serbia: IEEE, May 2014, pp. 209–212, ISBN: 978-1-4799-5296-0 978-1-4799-5295-3 978-1-4799-5293-9. DOI: 10.1109/MIEL.2014.6842123.
- [7] L. Chrostowski, H. Shoman, M. Hamood, *et al.*, "Silicon Photonic Circuit Design Using Rapid Prototyping Foundry Process Design Kits", en, *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 25, no. 5, pp. 1–26, Sep. 2019, ISSN: 1077-260X, 1558-4542. DOI: 10.1109/JSTQE.2019.2917501.
- [8] *Lumerical Interconnect*. [Online]. Available: <https://www.ansys.com/products/photonics/interconnect> (visited on 05/04/2023).
- [9] *IPKISS Design Suite*. [Online]. Available: <https://www.lucedaphotonics.com/luca-da-photonics-design-platform> (visited on 05/04/2023).
- [10] F. Laporte *et al.*, "Highly parallel simulation and optimization of photonic circuits in time and frequency domain based on the deep-learning framework pytorch", *Scientific reports*, vol. 9, no. 1, pp. 1–9, 2019. DOI: <https://doi.org/10.1038/s41598-019-42408-2>.
- [11] J. Sepulveda, S. L. Beux, J. Luo, *et al.*, "Communication Aware Design Method for Optical Network-on-Chip", en, in *2015 IEEE 9th International Symposium on Embedded Multicore/Many-core Systems-on-Chip*, Turin, Italy: IEEE, Sep. 2015, pp. 243–250, ISBN: 978-1-4799-8670-5. DOI: 10.1109/MCSoc.2015.33.
- [12] T. Ferreira De Lima, A. N. Tait, A. Mehrabian, *et al.*, "Primer on silicon neuromorphic photonic processors: Architecture and compiler", *Nanophotonics*, vol. 9, no. 13, pp. 4055–4073, 2020. DOI: <https://doi.org/10.1515/nanoph-2020-0172>.
- [13] P. J. Ashenden, *The designer's guide to VHDL*. Morgan Kaufmann, 2008. DOI: <https://doi.org/10.1016/B978-0-12-088785-9.X0001-9>.
- [14] E. Christen and K. Bakalar, "Vhdl-ams-a hardware description language for analog and mixed-signal applications", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 10, pp. 1263–1272, 1999. DOI: 10.1109/82.799677.
- [15] B. J. Shastri, A. N. Tait, T. Ferreira De Lima, *et al.*, "Photonics for artificial intelligence and neuromorphic computing", en, *Nature Photonics*, vol. 15, no. 2, pp. 102–114, Feb. 2021, ISSN: 1749-4885, 1749-4893. DOI: 10.1038/s41566-020-00754-y.
- [16] S. Rumley, M. Bahadori, K. Wen, D. Nikolova, and K. Bergman, "PhoenixSim: Crosslayer Design and Modeling of Silicon Photonic Interconnects", en, in *Proceedings of the 1st International Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems - AISTECS '16*, Prague, Czech Republic: ACM Press, 2016, pp. 1–6, ISBN: 978-1-4503-4084-7. DOI: 10.1145/2857058.2857061.
- [17] J.-J. Crespo, F. J. Alfaro-Cortés, and J. L. Sánchez, "PhotoNoCs: Design Simulation Tool for Silicon Integrated Photonics Towards Exascale Systems", en, in *Euro-Par 2017: Parallel Processing Workshops*, D. B. Heras, L. Bougé, G. Mencagli, *et al.*, Eds., vol. 10659, Series Title: Lecture Notes in Computer Science, Cham: Springer International Publishing, 2018, pp. 715–724, ISBN: 978-3-319-75177-1 978-3-319-75178-8. DOI: 10.1007/978-3-319-75178-8_57.
- [18] M. Briere, E. Drouard, F. Mieyeville, D. Navarro, I. O'Connor, and F. Gaffiot, "Heterogeneous Modelling of an Optical Network-on-Chip with SystemC", en, in *16th IEEE International Workshop on Rapid System Prototyping (RSP'05)*, Montreal, Canada: IEEE, 2005, pp. 10–16, ISBN: 978-0-7695-2361-3. DOI: 10.1109/RSP.2005.25.
- [19] *Specs repository*, <https://github.com/clement-z/specs>.
- [20] *SystemC standard*. [Online]. Available: <https://systemc.org> (visited on 05/04/2023).
- [21] *KiCad*. [Online]. Available: <https://www.kicad.org/> (visited on 05/04/2023).